

Fig.1

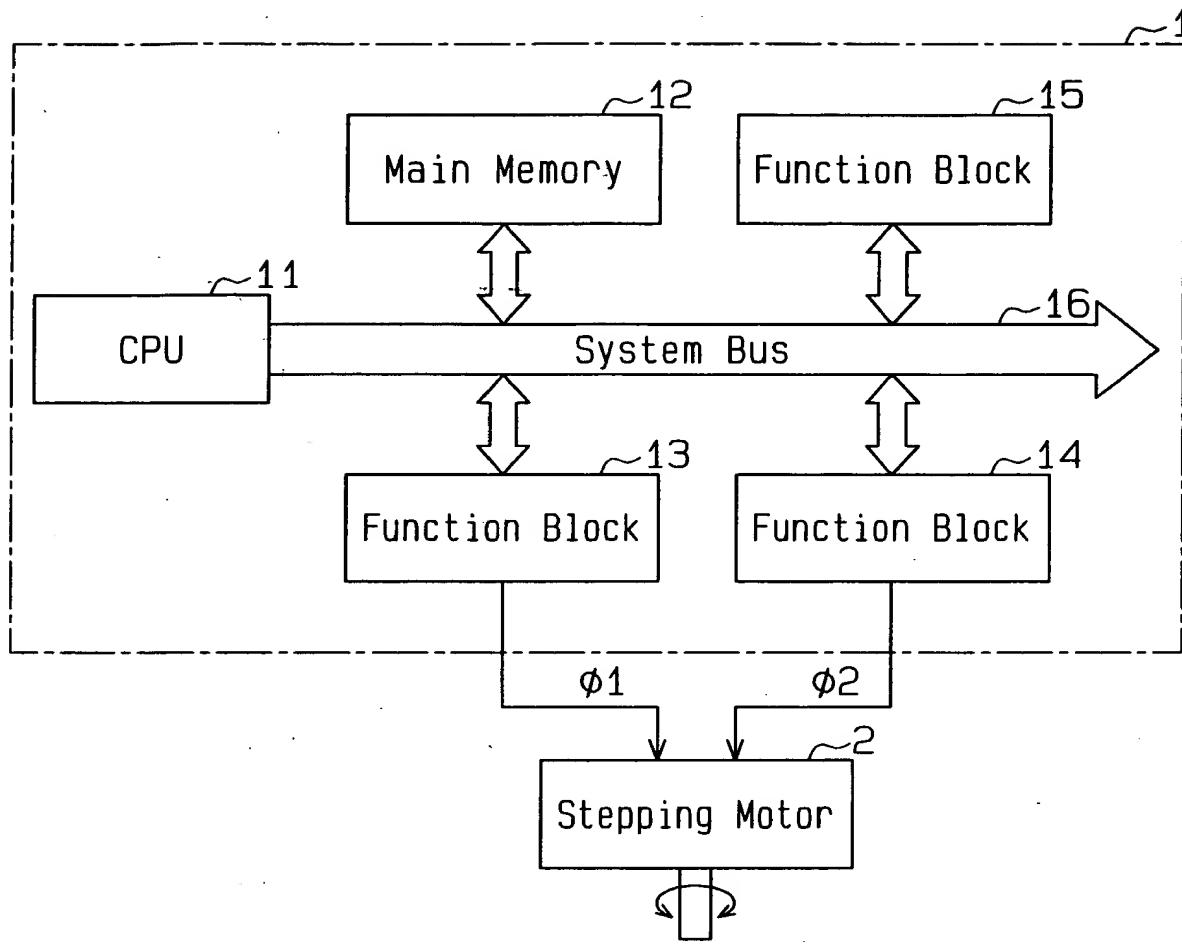


Fig.2

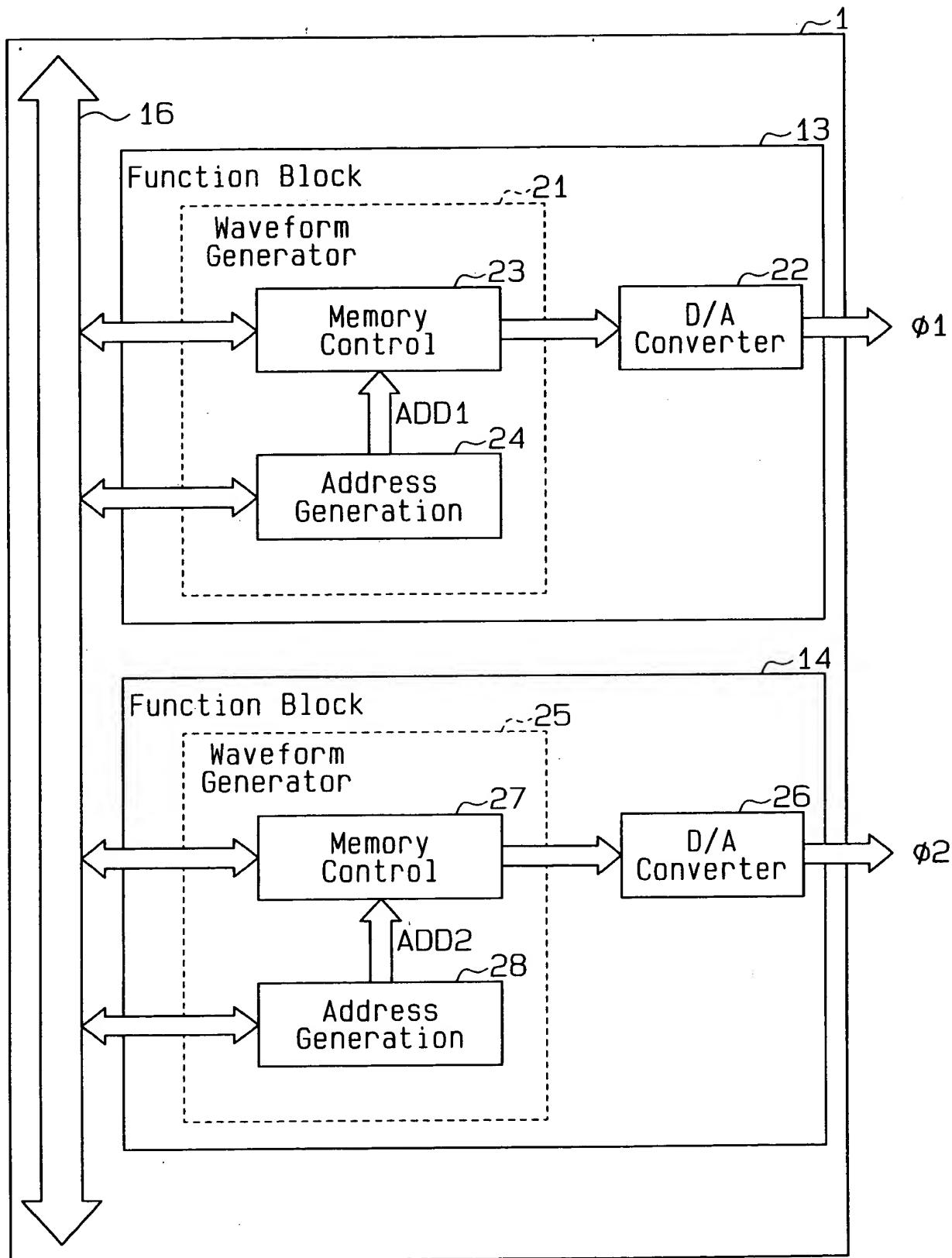


Fig. 3

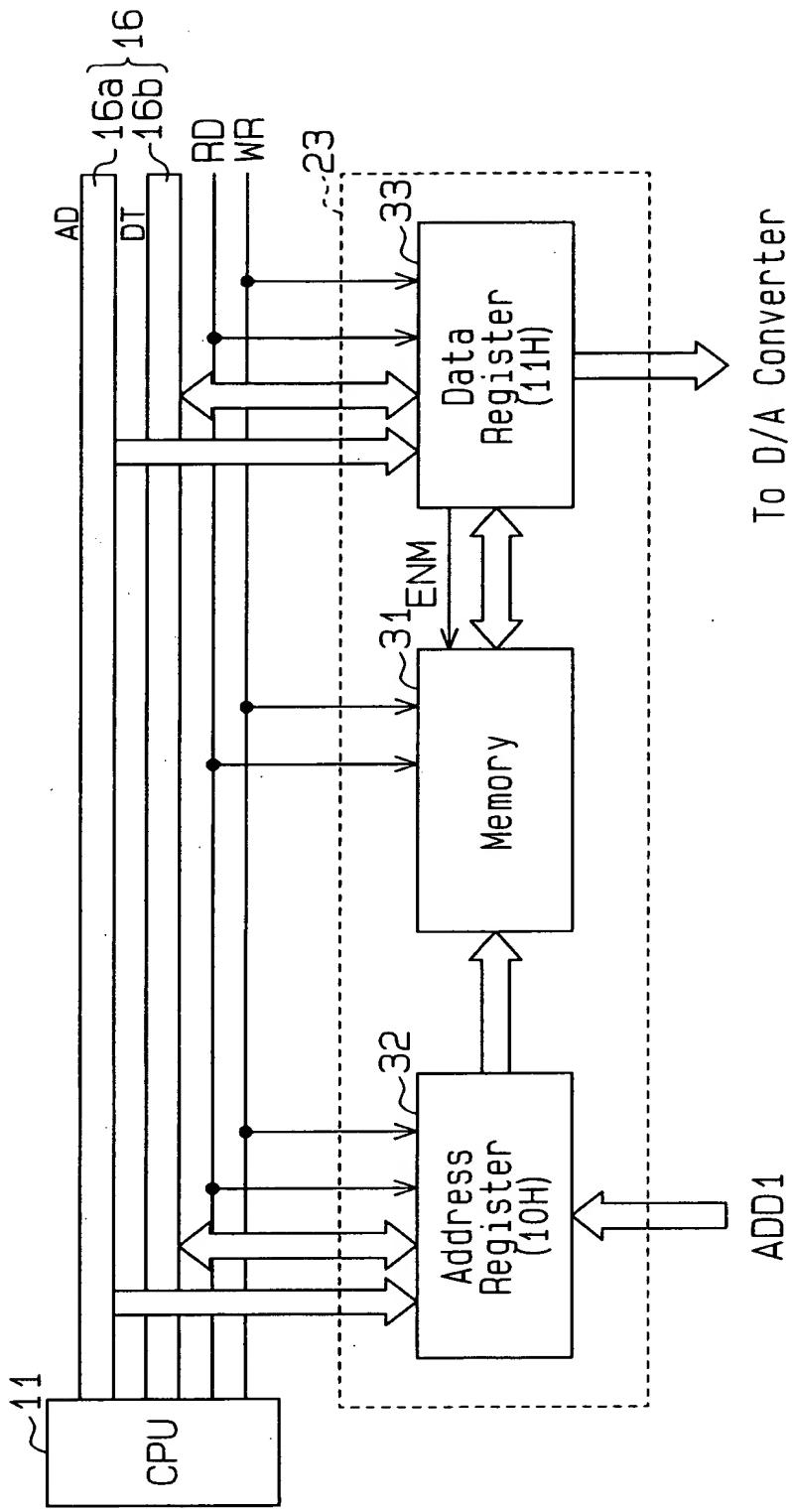


Fig.4

	Cycle	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
CPU	AD	X00	X00	X10	X11	X10	X11	X10	X11	X00	X00	X00	X	
	DT	X00	X00	X00	X80	X04	FF	X04	FF	X00	X80	X10	X55	XAX
	RD													
	WR													
Address Register	Register Value	XX	X00	X04		X00								X
Memory	Address	XX	X00	X04		X00								X
	Data	XX	X80	XX	FF		X80							X
Data Register	Register Value	XX	X80	XX	FF		X80							X

Fig.5

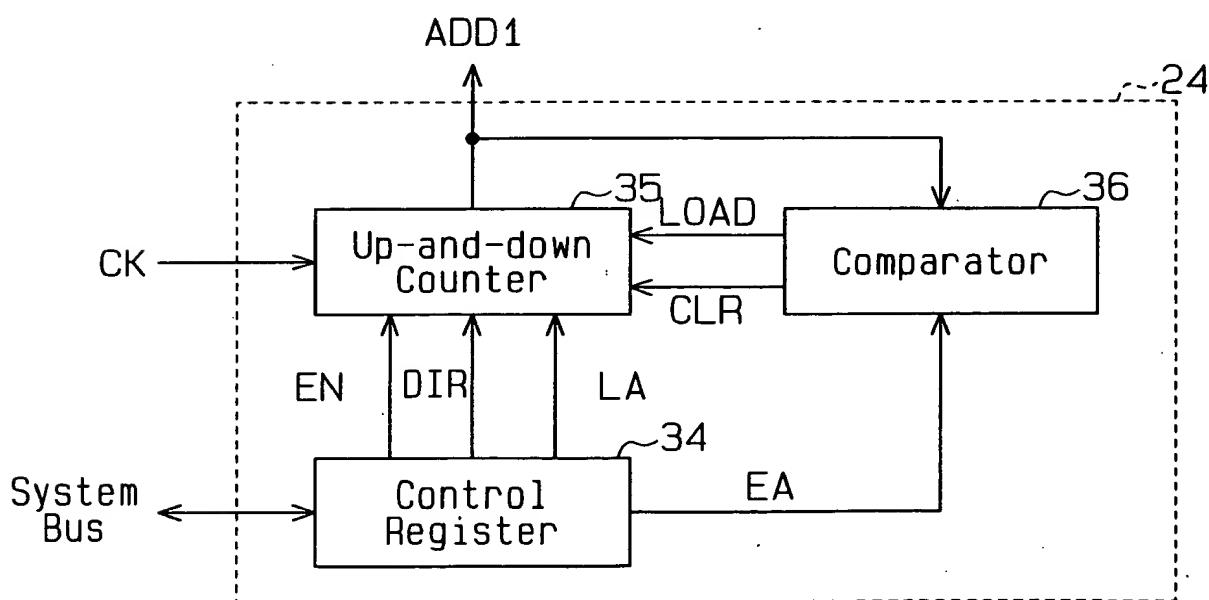


Fig. 6

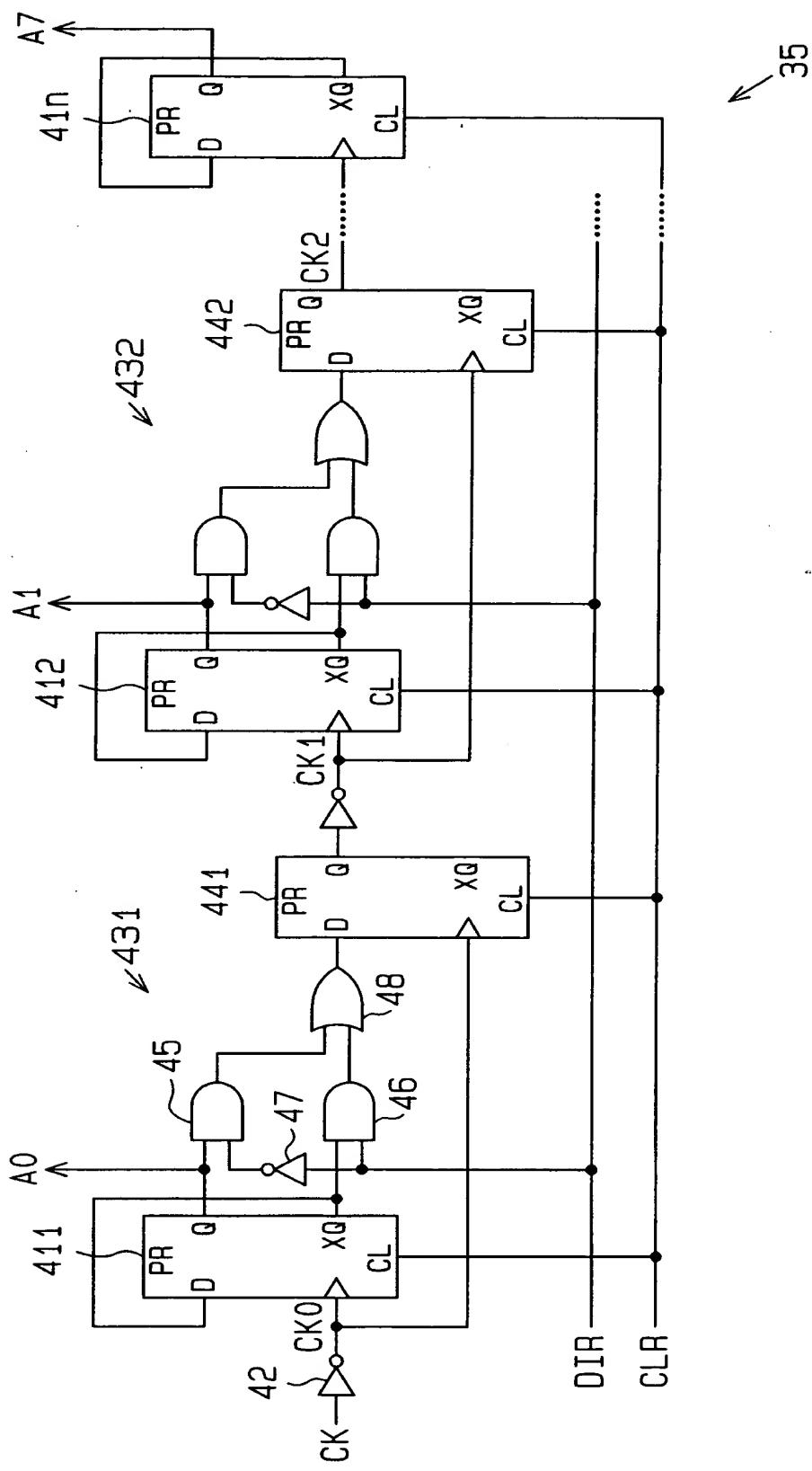


Fig.7

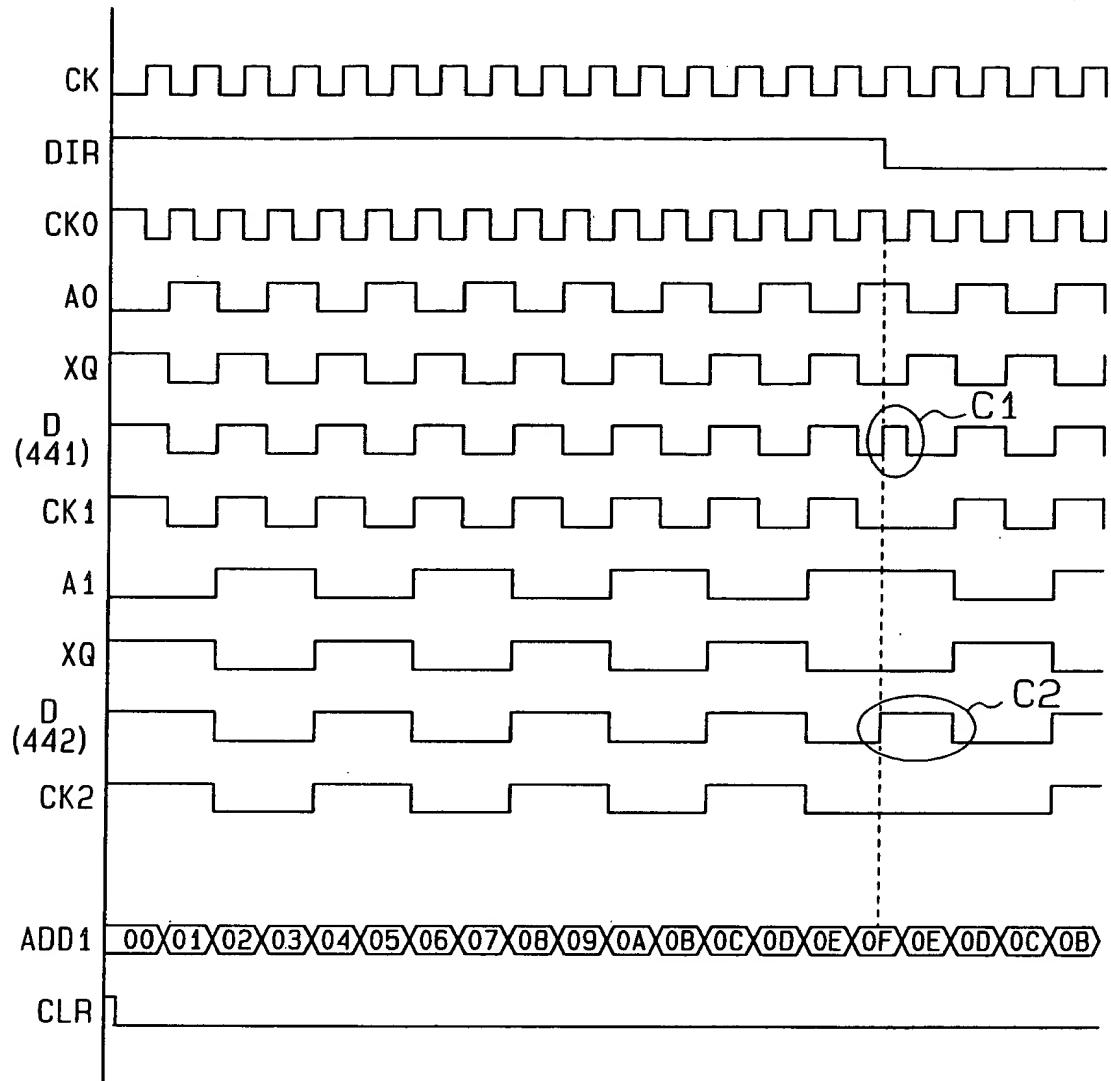


Fig.8

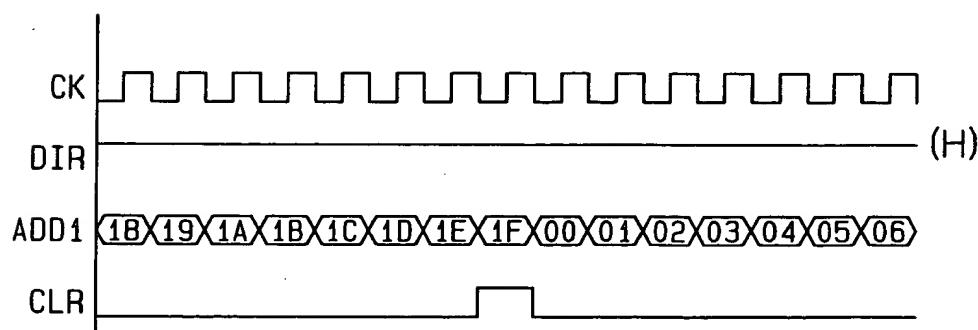


Fig. 9

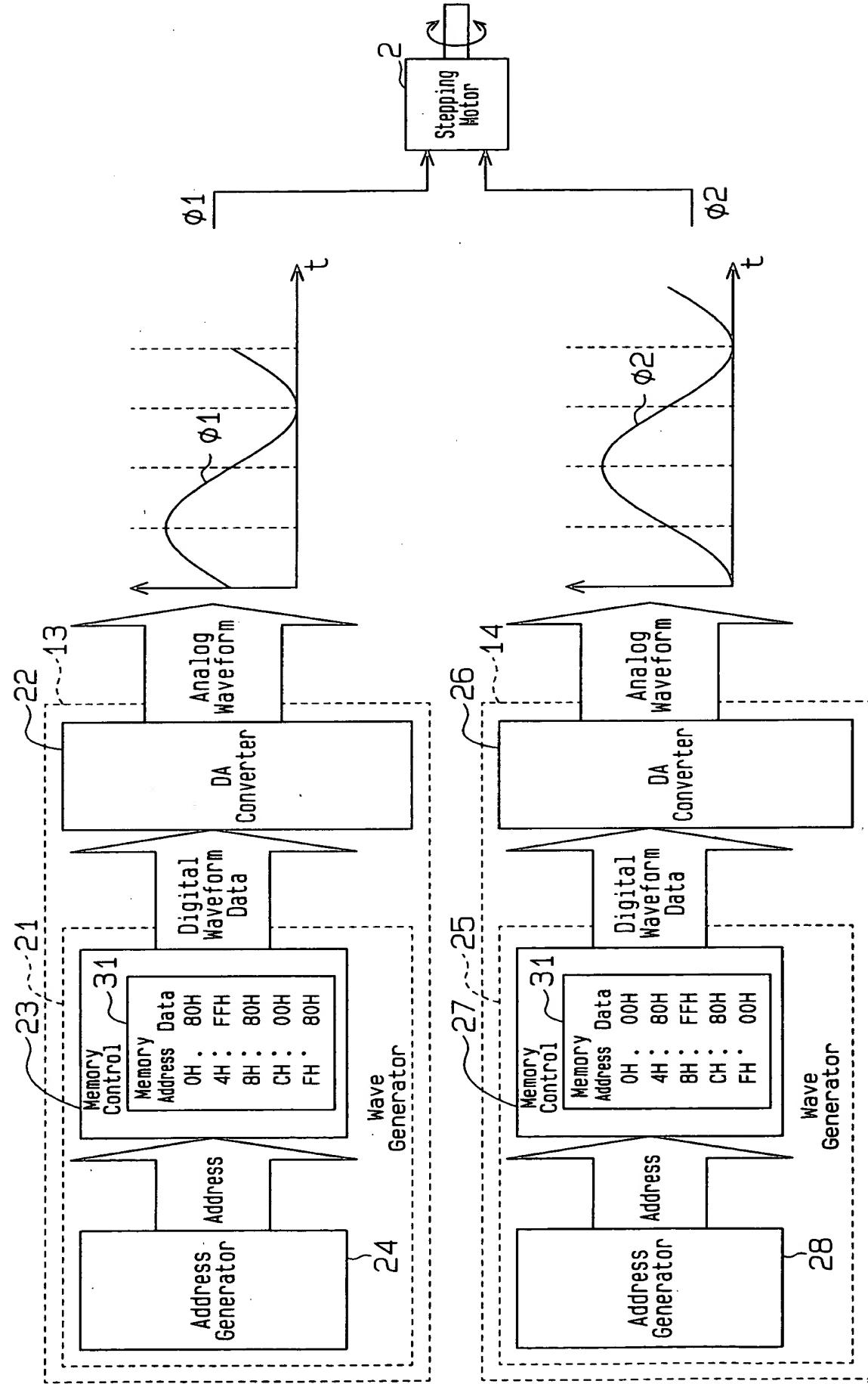


Fig.10

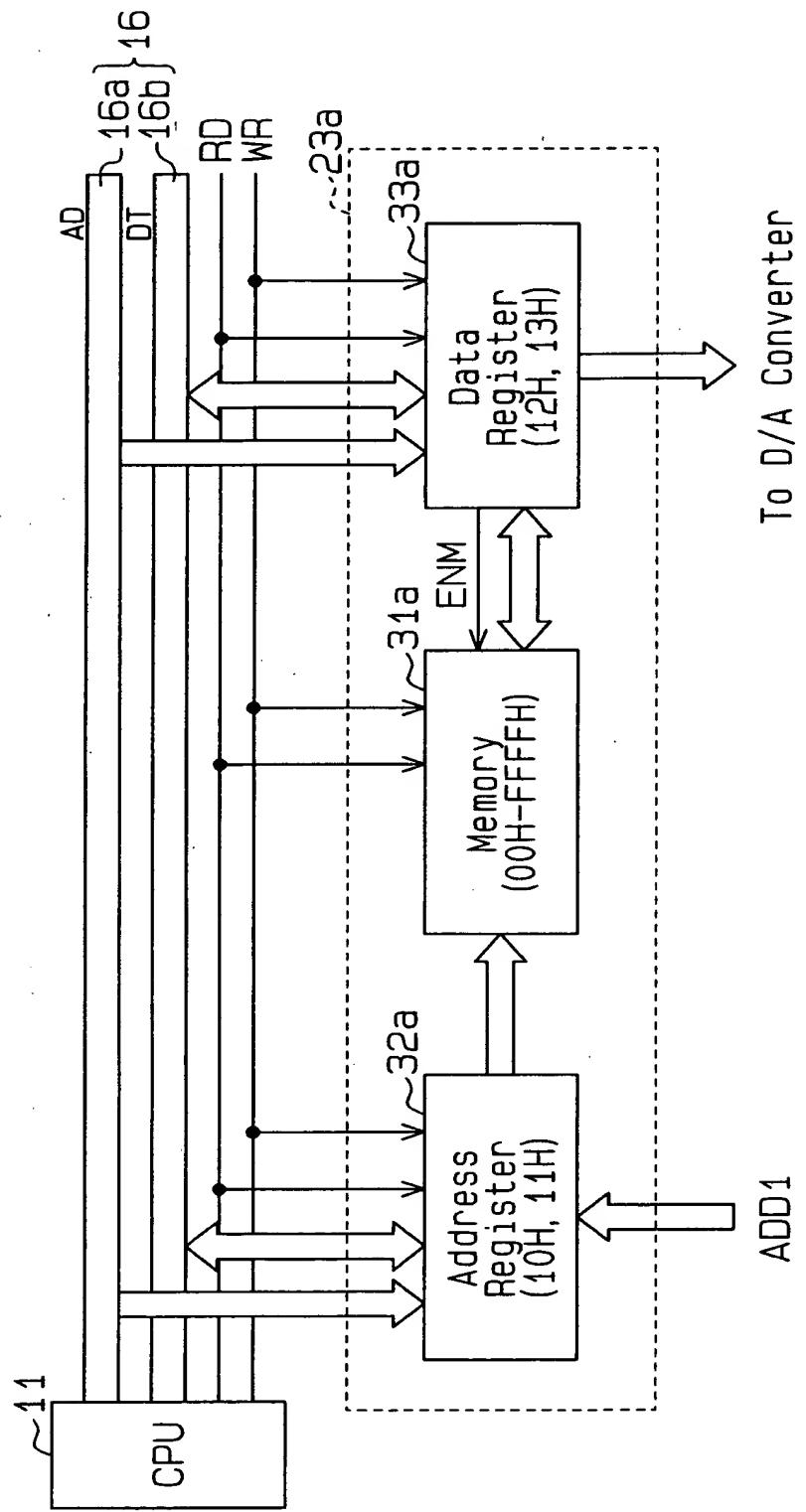


Fig. 11

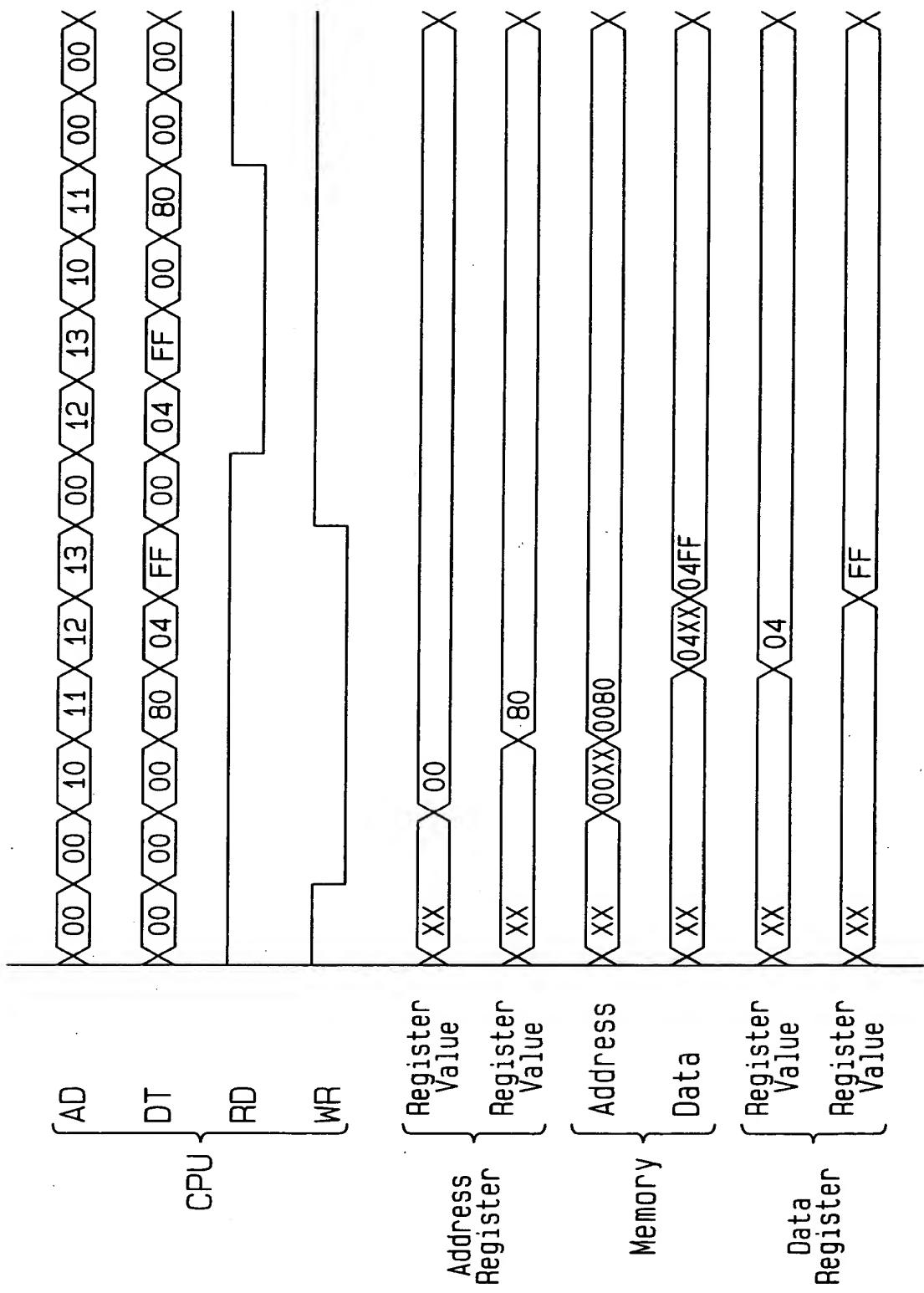
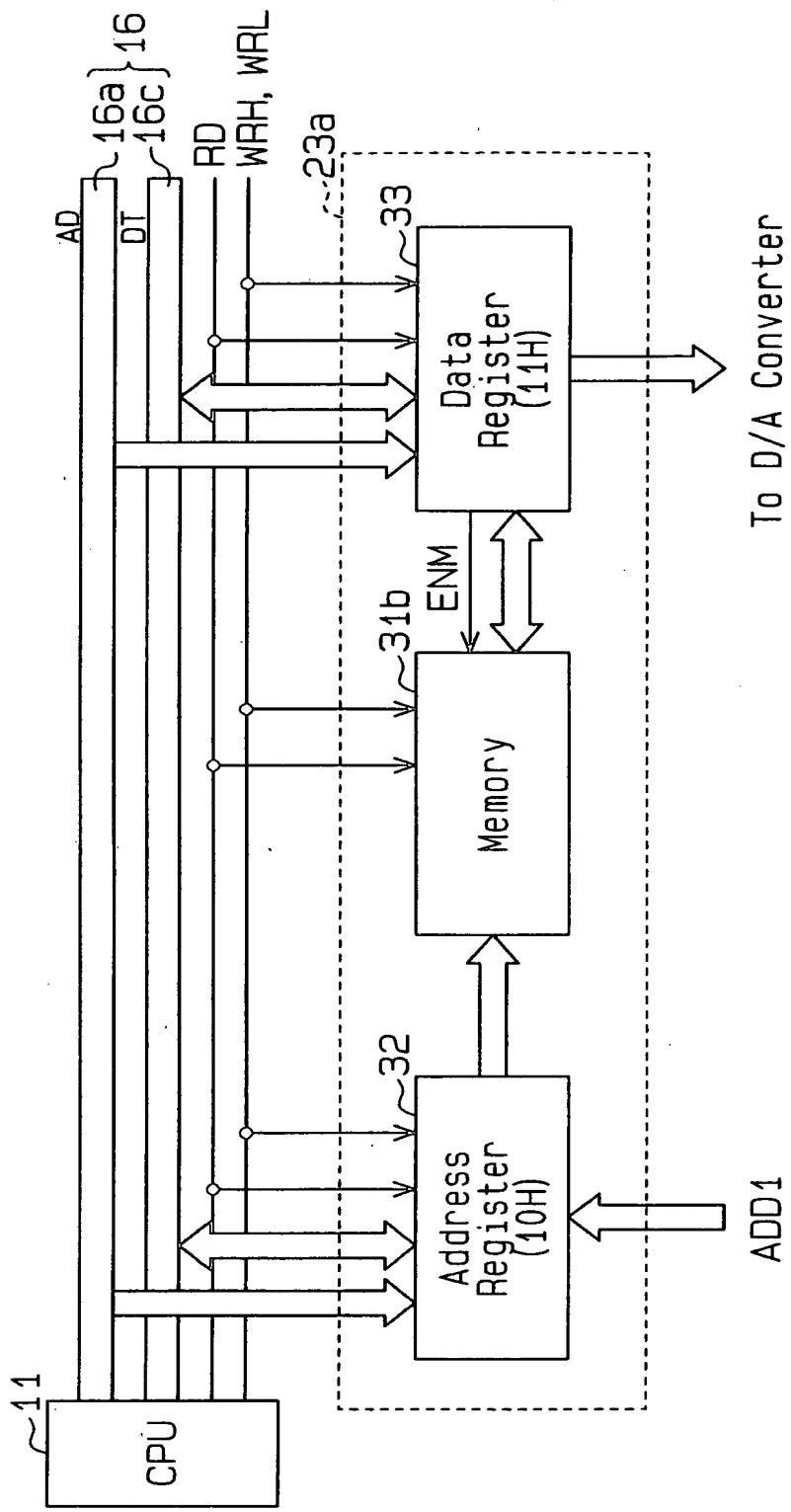


Fig. 12



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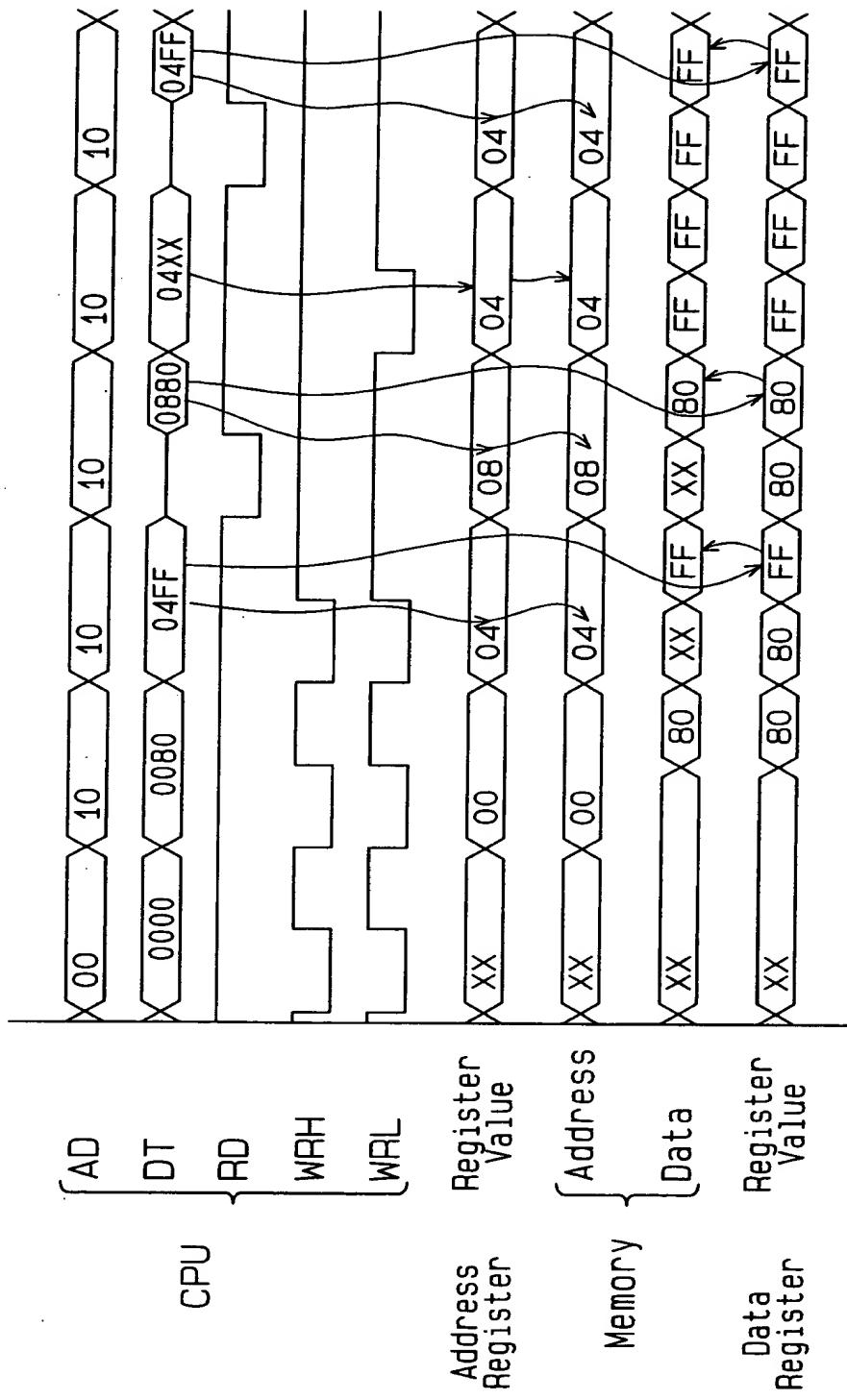


Fig. 14

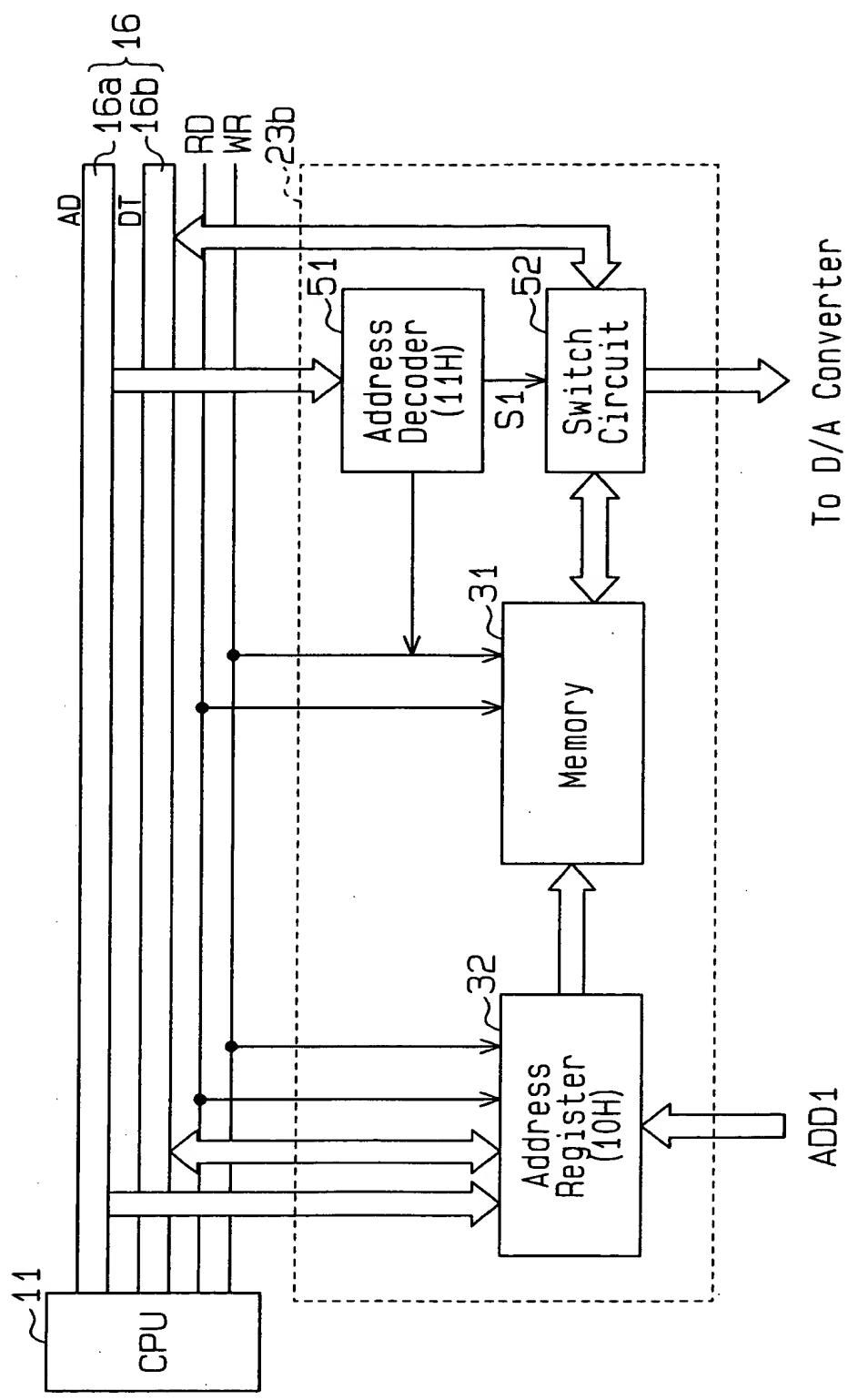


Fig.15

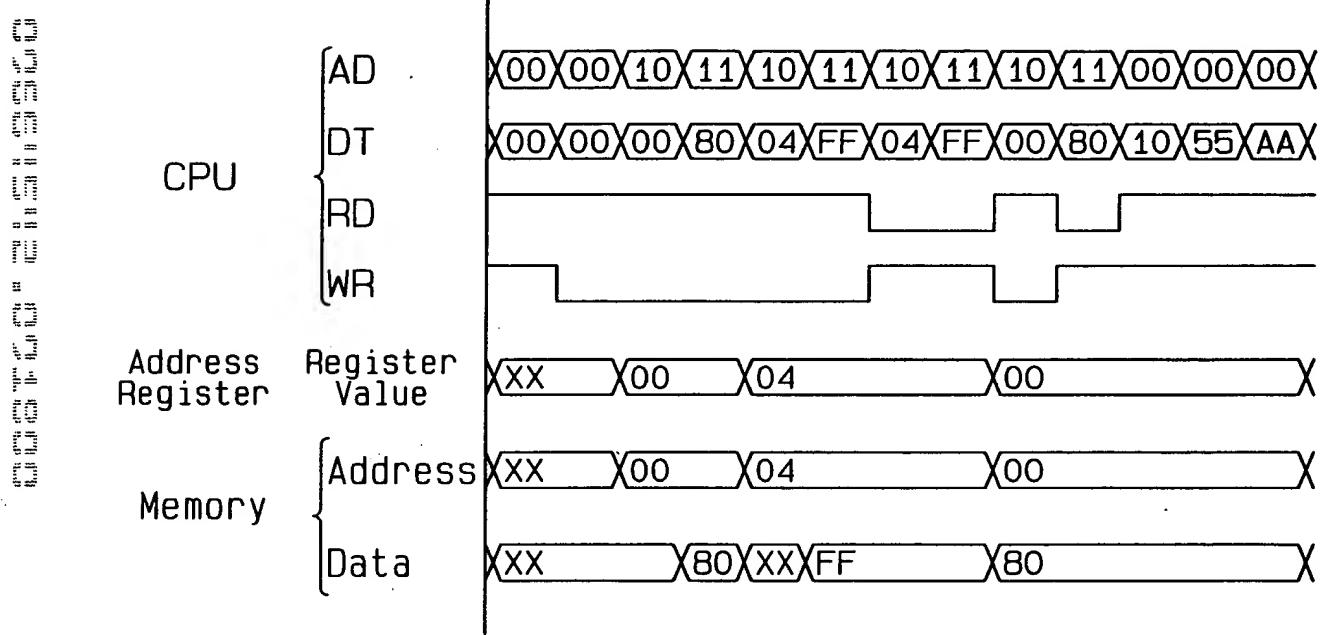


Fig. 16

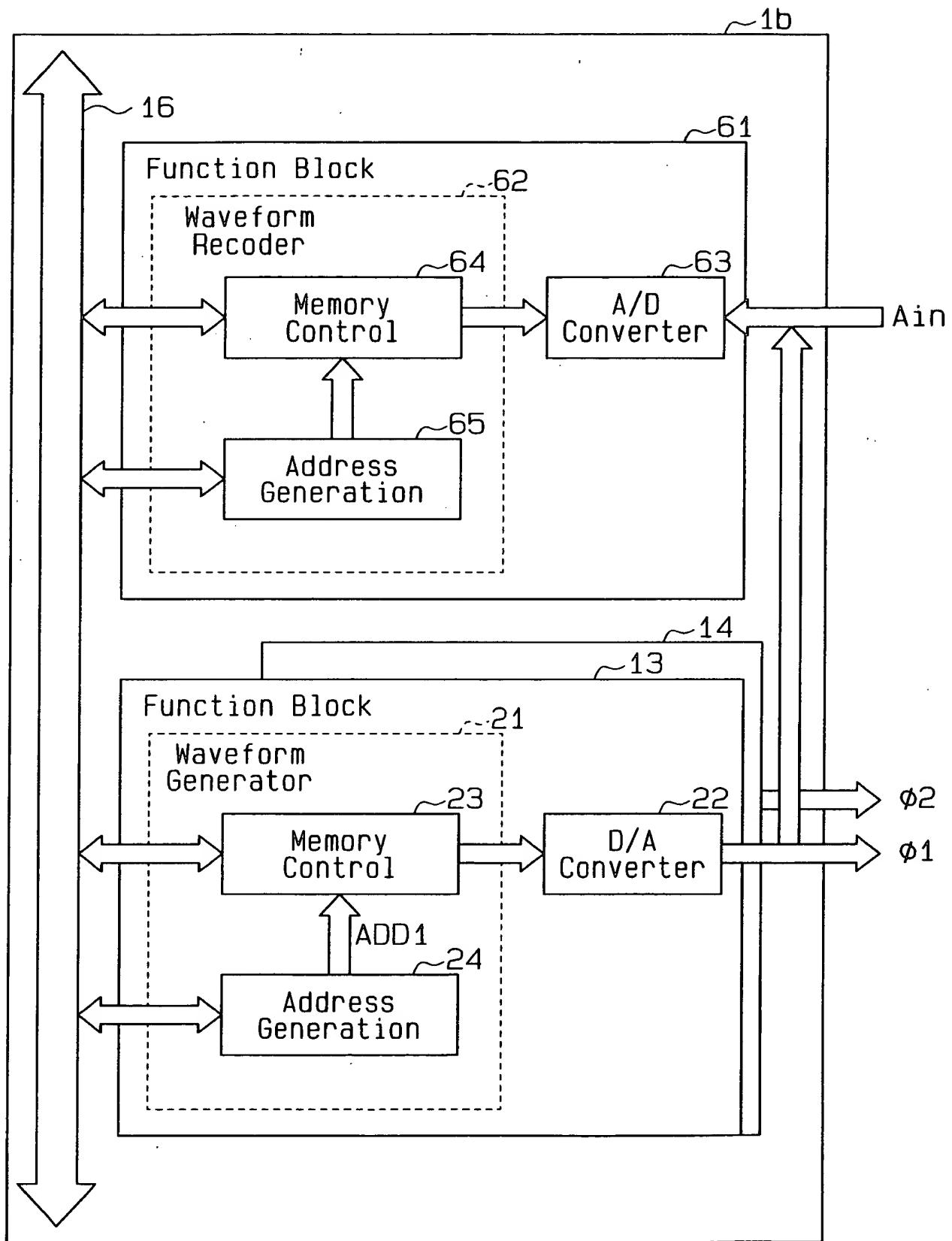


Fig.17

